PORTABLE ON-BOARD-DIAGNOSTIC (OBD) II / CAN SCAN TOOL

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Abstract

Today’s laws require that specific diagnostic information be made available on all vehicles manufactured on or after 1994 and sold in the United States. This information is typically available to a portable test device (Scan Tool) that is by necessity, external to the vehicle under test. Since this tool is not a part of the vehicle, it’s very nature indicates that it should be portable and battery operated. Usually it is connected to the test vehicle's required female J1962 connector. The interface must conform to the standard pin assignments as designated by the appropriate SAE document.

This white paper presents a design for a portable OBD II scan tool incorporating CAN and J1850 that is low enough in cost for the home or “shade-tree” mechanic to purchase. Because of all the regulations conformance requirements, etc., a detailed system is not presented, but a comprehensive engineering overview is. In the conclusion a list of references used in preparing this paper is available to allow readers to further research the requirements and other pertinent details required to implement a Scan Tool Design.

Figure 1: Possible OBD II implementation
In this design, extensive usage is made of many of the features incorporated in the Siemens SAB-C167CR-16FM 16-bit microcontroller (figure 4). Usage is made of the integrated 1 megabit capability on-chip full CAN (Controller Area Network) controller to process CAN messages.

Current US regulations requires that all vehicles make legislated diagnostic information available to external diagnostic tools via on board J1962 connector. Information at this connector is (as legislated) in the J1850 format as defined by the SAE (Society of Automotive Engineers) recommended practice, J1850. The current CAN interface as currently proposed contains all of the required information and will be available on the J1962 connector.

Design Parameters (please see Fig. 2)

The J1978 specifies that when a diagnostic tool is plugged into the vehicle's J1968 mating connector and/or OBD II support is selected a test of all the OBD II communication interfaces is to be performed once per scan. The scan should be continued until either successful or terminated by the user.

The instrument can be put in a “baby-sitting” mode and when the appropriate
trigger message appears it will turn on an
annunciation and possibly also close a set of
isolated contacts.

Note: currently CAN is not part of
the existing diagnostic network, but only a
recommendation. Currently the actual CAN
implementation is still to be determined.

This design as presented here allows
several hundred messages to be stored in the
tool's memory. This information will be
made available to other programs when the
tool is connected to a PC or other
instrument. This will allow an elaborate
diagnostic display to be generated. The
information acquired from the vehicle can be
used to make inquiries into a data base and
possibly lead the mechanic directly to the
problem.

The cost of this system is intended to
be low enough in cost for the average home
mechanic to purchase. Only A PC is
required to update the internal 128K Flash
EPROM. If the user does not have a PC, the
update can take place at the retailer in a few
short minutes.

If the user does have a PC, extensive
diagnostic and trouble shooting information
can be made available in text and / or
graphic presentations. Because of the
amount of memory available in the typical
PC a very comprehensive data and diagnosis
data base can be made available to the user
allowing simplification of the diagnostic
procedure and possibly even recommending
appropriate replacement parts.

The diagnostic software for the PC
can be made available as an option,
increasing revenues for the retailer, and
saving money for users that do not need or
want the extended diagnostic capability.

This capability will also be extended
to vehicular systems that are implementing
CAN as the vehicle network. The
information can be presented by the internal
CAN bus or via a gateway depending on the
manufacturer's preference. Please note that
the current J1850 specifications are severally
band width limited when compared to CAN
and its capabilities. J1850, a class "B"
network tops out at about 125K baud,
CAN tops out at 1,000K baud, about eight
times faster. The actual throughput is
controlled by the format used by the
messages and the efficiency of the messages.

In addition to the J1850 (includes
ISO 9141-2) interface a CAN interface is
also provided as currently proposed in the
SAE practices. This will give the user even
more information, benefits, and diagnostic
information. There is no CAN connector
currently supplied or specified for general
diagnostic usage at the present time. The
current recommendations are that pins 6 and
14 of the J1962 connector be dedicated for
the CAN interface to the external OBD II
scan tool.

Because it is possible to damage the
physical interface, and it is also likely the bus
or message specifications can change the
Physical Layer devices (J1850, CAN, and
PC) are located on a plug in the daughter
board.

The display is shut down after a
period of time of inactivity to help conserve
battery life. Shutdown would normally only
be active if the instrument is operating from
its internal batteries. The user has the option
of enabling or disabling this function.
The Power Supply (please see fig. 3)

The power supply is critical to the hand held scan tool. It must be reliable, robust, and occupy a small area of the system. In the design all components are SMT (Surface Mount Technology), keeping the physical PCB (Printed Circuit Board) area quite small. Protection is provided for reverse battery connection as well as load dump conditions that may occur.

Figure 3: Power Supply Schematic

The tool as presented here will run powered from the vehicle under test, wall mount transformer or its internal battery. Battery power is supplied by the internal Ni-Hydride battery. This battery is rechargeable and is charged either from the wall mount transformer or the vehicle while scanning.

Recharging is automatic any time the tool is connected to the vehicle unless battery voltage is low or it is commanded otherwise. The battery will always charge when connected to the wall transformer. The J1962 connector is specified to supply a maximum of four amps to the testing device at a nominal voltage of 14.4 Volts DC.

If the vehicle’s battery voltage falls below either a predetermined voltage (controlled by software) or a programmable set point, the tool will issue a warning to the operator informing him that the system is about to shut down.

The on-board microcontroller SAB-C167CR-16FM using one of its sixteen internal 10-bit (9.7uS @ 20Mhz) Analog to Digital Converter (ADC) channels, monitors the voltage supplied to the J1962 connector by the vehicle under test. If the voltage is below 12 volts (indicating that the vehicle is running on battery power only), the microcontroller will not charge the tools internal battery from the vehicles electrical
system, thereby minimizing demand on the test vehicle. Because of the tool's low power consumption, enough energy can be drawn from the vehicle to charge the scan tool's internal battery as well as supply the necessary energy to keep the tool in operation.

The SAB-C167CR-16FM also monitors the charge condition of the internal battery with one of its ADC-channels and will start charging if enough energy is available from the test vehicle. Charging is accomplished by using a PWM (Pulse Width Modulation) technique.

Charging power (energy) is actually controlled by a small signal Siemens P-Channel enhancement MOSFET (BSP 171) connected through a current limiting resistor (10 Ohm) to the positive terminal of the battery. A zener diode is placed in the gate circuit of the BSP 171 to protect against load dump transients.

Voltage translation for the high side switch is provided by a small signal BSP 123 N-Channel enhancement MOSFET. The BSP 123 has a 1K resistor in series with its gate to control rise and fall times, minimizing radiated and conducted interference. The 5.6K resistor guarantees that the MOSFET turns off when the PWM input from the SAB-C167CR-16FM is in a tristate mode.

There is a 22 Ohm resistor in the source lead of the BSP 123 for load dump protection. It works simply by changing the enhancement point of the MOSFET as the current increases, placing it into a constant current mode.

As the $V_{BAT}$ voltage rises, current through a 22 Ohm resistor increases causing the voltage drop, across the 22 Ohm resistor, to increase. As this voltage increases, it decreases the gate to source voltage by an identical amount. This happens because the gate is driven from essentially a constant voltage source (output pin of the SAB-C167CR-16FM) which is connected to a regulated $5V_{DC}$ supply.

The MOSFET will hold off over 80 volts, the maximum voltage that the load dump would produce if the MOV failed. As soon as the load dump transient has dissipated, operation returns to normal, without any detrimental effects on the scan tool.

Reverse battery protection is provided by diode BAX 280. This is a 3.5A surface mount diode. If this diode is eliminated, the TLE4261 will also provide reverse battery as well as load dump protection for the logic circuits. Input rush current is limited in the power switch by a 1 Ohm resistor. This may be required for some switches because of the high inrush current, the $220\mu F$ capacitor will draw when the switch is first turned on. Additional advantage is an increase in the life of the switch contacts.

The Siemens TLE4261 was chosen because it is a very low drop out voltage regulator and the TLE4261 has many inherent features that make it ideal for portable or battery operated equipment. Its very low quiescent current along with the low starting current consumption extends battery life.

If batteries are inadvertently installed backwards the TLE4261 is designed to protect its load from reverse polarity. It will with-stand 42 Volts input with a surge capability of 65 Volts ($400\,\text{ms}$).

As expected, and required, short circuit protection and thermal protection is provided for system integrity and reliability.
The TLE4261 is the ideal location to generate the system reset because it monitors the incoming voltage and allows setting of the reset delay externally.

A watchdog circuit is also provided. In this application it is used as a redundant watchdog as the SAB-C167CR-16FM also contains an internal watchdog.

The TLE4261 is available in a space saving P-DSO-20-6 SMT package as well as a TO-220 package.

**Memory, External - Internal**

The 16-bit wide configuration saves the CPU an additional cycle every time external memory is accessed. The demultiplexed mode requires no additional external logic (such as latches, buffers, etc.) when external memory is addressed (see Fig.2). Internal RAM is accessed as 16-bit wide memory the same as external memory, while the internal 128K Flash EPROM is accessed as 32 bit wide memory. This 32 bit access improves the SAB-C167CR-16FM's core performance by approximately 30%.

Each memory block is not only provided with its own chip select, but all necessary wait states and other bus controls are automatically generated by the SAB-C167CR-16FM. The chip select range, wait-state(s) and other data is all under software control. Hardware control is implemented by programming the appropriate Special Function Registers (SFR).

This implementation allows the user to mix lower-cost, slower devices with faster devices such as RAM in a socket-by-socket basis. Jumpers are provided to connect the RD# (OE#), WR#, FLASH programming voltage, and other appropriate signals to the memory device chosen. This allows the user to also mix devices as desired.

The SAB-C167CR-16FM contains its own internal 128K bytes FLASH and 4K bytes of RAM memory, therefore it is possible in most applications that external memory will not be required. The actual amount of memory required will be entirely up to the users implementation and code requirements. The basic interface and communications capability could actually be implemented in less than 1024 words of code memory when utilizing the SAB-C167CR-16FM.

Port 0 provides a 16-bit bi-directional data bus once the SAB-C167CR-16FM is initialized. Port 0 is also used to select the system startup configuration by adding a few pull down resistors. During reset Port 0 is automatically configured by internal hardware to the input mode. Each port pin of Port 0 is held high by a internal pull up device. Each port pin can now be individually pulled to a low level through an external pull-down resistor (approximately 8K depending on other connections to port 0).

The actual configuration (mode of operation) in which the SAB-C167CR-16FM wakes up is programmed by these external pull-down resistors. Since the resistors have not been switched out of the system, the specification for the pull-down resistors have to be looked up in the Siemens data book. If the default mode is required, no pull-down resistors are needed.

At the end of reset, the selected bus configuration will be written to the internal BUSCON0 register. The configuration of the high byte of Port 0 will be copied into the special function register (SFR) RP0H. This
read-only register contains the chip select and segment address information. If needed the user’s software can read this SFR and operate appropriately.

The Internal program / data memory is implemented as 128K bytes of Flash Memory. Why Flash? Flash technology has consistently improved and production volume is now bringing Flash costs down, making it feasible and practical to implement on the microcontroller chip.

High performance CMOS microcontroller key features:

- 16-bit CPU with 4 stage pipeline and jump cache
- 16 channel 10-bit A/D, 9.7µs conversion time
- 32 bit bus to internal 128K byte flash EPROM
- 500ns multiply, 1µs divide (interruptible!)
- 4K bytes internal RAM
- Watchdog - 16-bit programmable
- von Neumann address space, 16Mbytes
- 32 capture/compare channels
- 90% of instructions execute in 100ns at 20MHz clock based on four 16-bit timer/counters
- Register based architecture with multiple variable banks
- 4 channel PWM at 78KHz 8-bit resolution
- 100ns context switching enhances task processing
- Boolean arithmetic and bit processing
- 8/16-bit external, MUX/DEMUX bus modes with HOLD/A
- 5 general purpose 16-bit timer/counters
- 5 simultaneous bus modes, each with a chip select
- 1 USART and 1 SSC, SPI compatible; 625KBAud, async 5MBaud sync
- Interrupt response in 400ns, 50ns sample period
- 112 I/O lines, CAN (full, part B), PLL 5MHz ext. input
- Interrupt with 16 priority levels in each of 4 groups
- Interrupts serviced by cycle stealing DMA (PEC)
- 144 pin Metric Plastic Quad Flat Pack package

Figure 4: Functional block-diagram of the SAB-C167CR-16FM

Integrating non-volatile memory into a controller instead of having memory external to it, offers several advantages. For example, at high frequencies an internal bus
to an internal memory reduces EMI. Furthermore, an internal memory is space-saving. The on-board programming, especially with the current explosion of SMT designs, is very important. It allows the user to quickly erase the memory on the SAB-C167CR-16FM embedded controller and reprogram it with new / updated code and data. This can be accomplished with minimal design impact, and the programming can typically be accomplished with the same PC the designer is using to generate the code.

The programmability is built into all systems with the on-chip Boot-Strap-Loader using the serial interface.

This allows the Flash memory to be changed externally and easily, (erased and programmed) making it a very viable solution for system debugging and field upgrades. The flexibility of the on-chip Flash memory typically eliminates the need for additional components and the associated PCB area reducing the size of the end product and increasing the functionaries verses cost ratio. Flash makes field software upgrades very simple and reliable.

The Keyboard

The keyboard shown (Fig. 1) contains 15 keys and as shown in Fig. 2 could be extended up to 256 keys, more than enough for most tool configurations. Each of the two 16 bit ports are pulled down with 10K resistors. These pull-down resistors will allow the software to scan in any order and detect multiple key depressions as well as allow a fast scan mode (~200ns). The fast scan mode is implemented by simply reading the “row-port”. If the value returned by the “row-port” read is zero, then no key is currently pressed.

The SAB-C167CR-16FM’s high speed (100ns instruction-cycle at 20MHz CPU-clock), continually scanning the keyboard in a classical manner, will cause a lot of EMI interference to be generated unless extensive / expensive precautions are taken. With this in mind the hardware is designed to minimize the amount and volume of scanning required to detect a key closure.

This reduction is accomplished where the “row-port” will normally be in the high impedance input mode (pulled down) and the “column-port” will be in the active high state (output = 1).

One simple jump-if-zero- instruction based on the value contained in the “row-port” would be the equivalent of scanning all 256 keys. Any key closure will cause the appropriate bit in the “row-port” to go to the logic “1-state”, causing the port input value to become not-zero.

Obviously, if other keyboard configurations are used, masking will have to be implemented, but the reduction in EMI will be the same. This high speed scanning is accomplished without changing the state of any of the external keyboard lines, yielding the desired effect of minimizing and eliminating unnecessary EMI radiation.

With this design the only physical keyboard scanning required will be when a key-pressed is detected and it is necessary to determine which key has been activated. This scanning can be accomplished with any of the free 16-bit ports or partial ports of the SAB-C167CR-16FM depending on the desired key matrix and port availability.

The Display
The display is comprised of Smart LED display modules driven with the Synchronous Serial Communications (SSC) port of the SAB-C167CR-16FM which runs up to 5MHz transmission speed when utilizing a 20 MHz clock. Display dimming in this application is controlled by a simple command to the display. If other displays are used, dimming can be very simply accomplished by using one of the internal 32 PWM-channels with 400ns resolution or even with one of the 4 PWM-channels with 50ns resolution of the SAB-C167CR-16FM.

The SAB-C167CR-16FM is responsible for all message patterns displayed. In this implementation the Smart LED’s are not responsible for decoding data and converting it into displayable information. This was implemented in this manner to allow any symbol desired to be displayed while only being limited by the display organization.

The SAB-C167CR-16FM converts the data to be displayed to a bit pattern that relates to the display LED’s in a 1-to-1 relationship and sends it directly to the display. The load-line is then toggled and the display data for the commanded line is transferred to the output drivers for the selected row which in turn illuminate the appropriate LED’s.

Ambient light can be monitored with a photo cell connected to an analog to digital input of the SAB-C167CR-16FM. This information can be used to select the appropriate dimming level. Dimming level determination can also be based on power source as well as battery levels.

By SAE recommendation there must be enough display to show at least two messages concurrently on the instrument display. There is no limitation on the maximum number of valid messages that can be displayed. The recommendation is open in that it allows the designer to implement the number of message displays the application requires and / or the designer desires.

Although not implemented in this tool, there is no restriction that states graphic with a mixture of text and / or graphics only cannot be used. This tool actually supports a self contained limited graphic set (display limits) on the tool display itself. The tool is more then capable of supporting a full and comprehensive set of graphics on an external PC or other appropriate display system. This capability is also inherent if the self contained display is configured to support the appropriate graphic display information.
J1850

General

It is the intent of the J1850 network to interconnect different electronic modules on the vehicle using an "Open Architecture" approach. An open architecture network is one in which the addition or deletion of one or more modules (nodes) has minimal impact on the software and remaining modules. Modules in this intent also include an external scan tool that conforms to all of the SAE recommendations as well as have the necessary capability to conform to future recommendations. Part of the future would be CAN and the appropriate interfaces and information that would become available to the scan tool.

In order to support an open architecture approach, the network utilizes the concept of Carrier Sense Multiple Access (CSMA) with non-destructive arbitration. This is valid for both the J1850 and CAN implementations. Additionally, the network will support the priority of frames such that, in the case of contention (arbitration), the higher priority frames will always win arbitration by the appropriate rule set and be transmitted completely without message destruction. The designer must take into account the “propagation-delays” generated in the physical layer with this setup.

Automotive multiplexing Class A (SAE), is defined for convenience operations and a data rate less than 10Kb/s, with a message rate around 100ms. Class B, is for most information transfer with medium speed data rate from 10Kb/s to 125Kb/s. The message rate is around 20ms. Class C, and / or CAN is defined for real time or critical control type applications. It has a high speed data rate of 125Kb/s to 1Mb/s or greater. The message rate is in the range of 5ms.

Mux Bus Control

This Class B network is a non-destructive bit-by-bit arbitration bus protocol, and is intended for a "master-less" bus control.

The principal advantage of master-less bus control is its ability to provide the basis for an open architecture communications system. The "master-less" bus control concept is ideally suited for data that is characterized as non-periodic, and event driven. In theory, since a master does not exist, each node has an equal opportunity to initiate a data transmission once an idle bus has been detected. Since, all modules and/or data frames are not of equal importance, prioritization of frames is incorporated with the highest priority frame always being completed. This implies correctly that frame / data-contention will not result in lost data.

The user must be aware that the specification describes two specific implementations of network, based on media physical layer differences. These physical layers are optimized for data rates of 10.4 Kbps while the other physical layer is optimized for a data rate of 41.6Kbps.

OSI Model

The OSI-model (Open Systems Interconnection) is broken down into seven layers. Only the physical & data link layer will be discussed here.

Physical Layer Overview
The layer provides for the transparent transmission of bit streams between data-link entities across physical connections, which is the interconnection path for information transfer between nodes. This layer is responsible for voltage, current, media impedance, bit/symbol generation and clock recovery. The requirements will be met by another device which the J1850 portion of the interface will communicate with.

The physical layer receives data from the bus and converts it to a sequence of ones and zeros which it presents to the data link layer. It also receives a sequence of ones and zeros for which it is responsible for converting to the proper voltage, current, and wave form to present to the J1850 bus. This layer is specified as it would be detected on the network media, not within any particular module or integrated circuit implemented.

**Physical Layer Contention**

Contention is defined as a situation whereby more than one module attempts to access the bus at the same time. Contention will be resolved in the state machine in such a manner that the highest priority message will always be transmitted.

While transmitting its symbol-stream of ones or zeros onto the bus, the “MAC-sub-layer” (see OSI Model) concurrently monitors the bus. The bit-by-bit arbitration facilities of the “MAC-sub-layer” always resolves the conflicting bus signaling requests. This way a module detects a conflict in its access to the bus from one or more modules competing for the bus (contention). When a module receives a different bit from the bus than the one it is attempting to transmit, it immediately terminates the transmission of any further data or bits, but keeps listening. Since, all modules receive all frames, the received data is not lost by the contention resolution.

**Physical Layer Bit-by-Bit Arbitration**

The defined bit-by-bit arbitration homogeneously settles the conflicts that occur when multiple nodes access the bus while maintaining data integrity. The bit-by-bit arbitration is applied to each symbol/bit of the frame, starting with the SOF (Start Of Frame) symbol and continuing until the EOF (end of the frame).

Bit-by-bit arbitration is heavily dependent on the use of the physical layer. The bus has two valid signal states labeled dominate and recessive. All bits and/or symbols are presented to the bus as a sequential combination of these two states.

If both the dominate and recessive states are presented to the bus concurrently, the resultant state on the bus will always be dominate. This allows the “MAC-sub-layer” of the transmitting module to non-destructively detect a signal state on the bus that is different from the state being transmitted by itself. If this difference is detected, it immediately ceases transmitting, and shuts off its drivers. By default, priority is thus granted to the module sending a dominate state signal over modules sending recessive state signals. This mode of operation also allows the dominate signal to continue with out any errors occurring or data loss due to arbitration. The data pattern arbitration is transparent. The highest priority message will always get through.
As each bit is transmitted, the “MAC-sub-layer” monitors the bus to see if the value it is transmitting is in fact being transmitted by the bus. If the value supplied by the “MAC-sub-layer” is not the same as the value actually appearing on the bus, the device recognizes that it has lost in contention with another device and discontinues immediately, holding off its attempt to transmit until the bus is once again idle.

In contention, a dominate state always wins out over a recessive state. Since the address is the value first supplied on the bus, the address with the greatest dominance (higher priority) will win in arbitration. The J1850 bus architecture is such that the greater priority a device has the higher the probability that it will gain access to the bus.

By the time this white paper is published, appropriate physical layer interface chips (driver(s) and receiver(s)) should be available. Because of the current availability and all of the requirements that have to be adhered to no Physical Layer circuit design is presented. There are several appropriate physical designs presented in the SAE documentation complete with descriptions which are mentioned here.

Data Link Layer

The primary function of the data link layer is to convert bytes to be transmitted into a sequence of ones and zeros that will be passed to the physical layer for transmission on the J1850 bus. This layer is primarily responsible for the parallel to serial conversion and serial to parallel conversion. This layer will be incorporated into the SAB-C167CR-16FM with several other layers as part of the J1850 interface.

Error correction will be accomplished by requesting a re-transmission of the message. Flags will be maintained in RAM to not only notify the main program if any errors have occurred but also the nature of those errors.

CAN

The CAN (Controlled Area Network) protocol was originally defined by Bosch in the mid-eighties. It is an advanced serial communication protocol which efficiently supports distributed control and multiplexing with a very high safety level. This bus is standardized by ISO/OSI and is designed to support a wide baud range up to and including 1 Mbaud. Typical applications can be found in not only automotive and industrial environments but many others as well.

CAN is now well established in the world market commanding a leading position for vehicle networking. Over the past few years a number of vehicle manufactures have abandoned their propriety protocols and have switched to the time proven CAN protocol.

Real time control especially between the engine and transmission cannot survive at current class “B” speeds, but must go to something much faster in the near future. The current solution is to use point to point wiring, but the complexity and size of the wiring harness is getting to the point that it is unwieldy to handle in production.

Several United States vehicle manufactures are currently considering CAN
and even have it on some prototype vehicles that are currently in use on the road. CAN and J1850 are similar in many respects but also are very different. Can and J1850 hardware normally is not interchangeable or compatible, consequently the vehicle must be designed with CAN in order to take advantage of its many advantages.

CAN is an asynchronous serial bus system containing one logical but typically two physical lines (see Figures 5 and 6). The structure is open, and does not contain master nodes or slave nodes. Two or more nodes are required for the system to operate. The number of nodes can be changed dynamically by adding or removing nodes from the bus either physically or logically. Changing the number of nodes will not disturb the communications of the remaining nodes. When adding or removing a node it is possible to cause an error on the bus but the protocol is rugged and recovers nicely.

The bus logic corresponds to “wired-OR” logic. Typically recessive bits are a logic “1” and dominate bits are a logic “0”. This is shown in Figure 5.

Recessive bits are always overwritten by dominate bits on the CAN bus by definition, this is what the arbitration is based on. This can be seen in figure 1 where any transistor that turns on drives the bus low, inhibiting the bus from being in the “1” or logic high state.

If multiple transistors are on, the bus remains in the logic zero state for as long as any of the transistors are turned on or in the “dominate state”. As long as no transistor is turned on, the bus is in the recessive state or logic “1”. This shows that the dominate “0” will over power the recessive “1” causing the bus to be in the dominate “0” state.

![Figure 5: The CAN Logical BUS](image)

![Figure 6: Showing a Vehicle CAN system](image)

Shown in Figure 6 is a typical vehicle CAN system containing several nodes. Depending upon the specification chosen, there can be from 26 to 32 nodes. All nodes shown can communicate in class A active and all are compatible with class B.
All nodes can arbitrate and communicate in 2.0A active mode, which uses the eleven bit identifiers for each message frame. Nodes A and N can also communicate in mode 2.0B Active, using 29 bit message frame identifiers while node “B” ignores all of the message frames that are sent in this mode.

The “ECU” node and “N” node are capable of communicating in Version 2.0B Active. The ABS node as shown is capable of communicating in Version 2.0A Active but is Version 2.0B passive. That states that it will tolerate the Version 2.0B messages but will just ignore them and not generate an error frame nor will they save the message. See the following information on error frames.

When a medium is chosen for the bus, it must be capable of transmitting the two states: dominate and recessive non-destructively. Typically the bus lines consists of a twisted pair of wires, which is then labeled “CAN_H” (Yellow). and “CAN_L” (Green). This twisted pair is then connected directly to each of the nodes on the bus or with a connector (T like configuration), whichever the designer chooses.

If a “T” like configuration is used, care must be used when selecting the stub length. The bus itself is terminated with a resistor at each physical end (2). This reduces reflections and improves the bus integrity. It is not advisable to put the termination resistor in any of the modules as if the system changes they may no longer be on the physical end of the bus.

Data is transmitted in the NRZ (Non-Return-to-Zero) format. To ensure exact synchronization of all bus nodes, bit stuffing is used. This states that during the transmission of a message a maximum (five) number of bits may have the same polarity.

Whenever this maximum (5) number of bits of the same polarity is exceeded the transmitter will automatically insert one additional bit of the opposite polarity into the bit stream before transmitting the remaining bits. This bit insertion will continue until the message is sent. The receiver also checks the number of bits with the same polarity (5) and removes the stuffed bits from the bit stream. This removal of bits is known as de-stuffing.
Optional Scan Tool to Host Communications

Communications between the scan tool and the optional host computer will be via a user defined serial or parallel link. In this implementation the serial link will be required when programming the Flash memory (on-chip boot-strap-loader which uses the serial interface) contained in the scan tool, but in all other instances identical information will be available on either port.

The scan tool must have the capability of filtering the messages, and discarding the irrelevant ones. Then when a valid message is received, it will process it accordingly.

The scan tool must also have the capability of asking for re-transmission of failed messages. When directed by the user, it will initiate transmission of message(s) on the bus and keep retrying to send them at a periodic rate as specified in the SAE specifications or by the user, which ever is greater. The user can also specify the number of tries the scan tool will transmit the message(s) until a request is satisfied or intervention is needed. The communications to the J1850 bus will typically remain autonomous to the user at all times.

Summary

Conformance to J1978

For a tool to be labeled "OBD II SCAN TOOL COMPATIBLE" or "CONFORMS to SAE J1978" it must pass conformance testing. Tools that do not pass these tests are not to be labeled. Validation of the conformance test is the responsibility of the scan tool manufacturer. The manufacturer has the option to be self-certifying. J1978 specifies that in order for the tool to be certified it must pass a series of tests that must be performed successfully, five consecutive times.

If there are any changes to the hardware or software used in the tool for the functions described in J1978, the conformance testing may have to be repeated with the modified tools. If the tools are sold, the manufacturer must make available the methods used to make these tests as well as the results therein. These must also contain a clear indication of the versions of hardware and software that is used in equipment labeled as confirming to or compatible with J1978. Copies of these tests, J1978 documentation as well as other documents can be obtained from SAE.
As far as patents or other rights of third parties are concerned, liability is only assumed for components per se, not for applications, processes and circuits implemented within components or assemblies.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design are reserved.

For questions on technology, delivery and prices please contact the Offices of Siemens Aktiengesellschaft in Germany or the Siemens Companies and Representatives worldwide.

Due to technical requirements, components may contain dangerous substances. For information on the type in question please contact your nearest Siemens Office, Components Group.

Siemens AG is an approved CECC manufacturer.

References

J1113
Electromagnetic Susceptible Measurements Procedures for Vehicle Components

J1211
Electronic Equipment Design Recommended Procedure

J1213
Glossary of terms for vehicle networks

J1547
Electromagnetic Susceptibility Measurement Procedures for CM Injection

J1850
Class B Data Communication Network Interface 4/94

J1879
General Qualifications and production Acceptance Criteria

J1930
E/E Systems Diagnostic Terms, Definitions, Abbreviations and Acronyms

J1962
Diagnostic Connector

J1978
OBD ii Scan Tool 3/94

J1979
E/E Diagnostic Test Modes

J2008
Recommended Organization of Vehicle Service Information

J2012
Recommended Format and Messages for Diagnostic Trouble Codes
J2186
Diagnostic Data Link Security

J2190
Enhanced E/E Diagnostic test Modes

J2201
Universal Interface for OBD II Scan Tools

J2205
Expanded Diagnostic Protocol

J2300
Conformance Test Procedures for OBD II Scan Tools

ISO 9141-2
Road vehicles Diagnostic Systems - CARB requirements for inter-change of digital information.

CAN Connective With The SAB-515C
Siemens Application Note by Gil Shultz and Axel Wolf

CAN Connective With The SAB-167CR
Siemens Application Note by Gil Shultz and Axel Wolf

Copies of these documents as well as other documents can be obtained from the appropriate source as listed below:

SAE
Society of Automotive Engineers, 400 Commonwealth Drive, Warrendale, PA 15096-0001

ISO, ANSI
11 West 42ns Street, New York, NY 10036-8002.

Siemens Components Inc.
Siemens Components Inc., Semiconductor Group, 10950 North Tantau Avenue, Cupertino, CA 95014

California ARB Documents
Title 13, California code of Regulations, Section 1968.1 Malfunction and Diagnostic System Requirements -- 1994 and Subsequent Model Year Passenger Cares, Light-Duty Trucks, and Medium-Duty Vehicles and Engines (OBD II).

Federal EPA Documents